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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,668	09/09/2003	Qi Xiang	039153-0675	1996
23392	7590	06/01/2005	EXAMINER	
FOLEY & LARDNER 2029 CENTURY PARK EAST SUITE 3500 LOS ANGELES, CA 90067			TRINH, HOA B	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/658,668

Applicant(s)

XIANG ET AL.

Examiner

Vikki H. Trinh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 14-32 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 14-32 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Acknowledgement

Claims 14-32 are pending in the present application.

Claim Objections

1. Claim 16 is objected to because of the following informalities: In claim 16, line 1, "claim 15" should be "claim 14", since claim 15 was canceled. Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 14-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Felker et al. (hereinafter Felker) (6,508,948).

As to claim 14, Felker discloses a method of making a semiconductor device having the steps of forming a silicon substrate 12 (fig. 1, col. 4, lines 3-5; col. 6, lines 61-62); forming a dielectric layer 22 on the substrate (col. 7, lines 1-5), forming a silicon carbide layer of the dielectric layer (col. 6, line 64; col. 7, lines 1-5); and bonding a second dielectric layer 22 (col. 6, line 64, col. 7, lines 1-5) on the silicon carbide layer.

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As to claim 15, the dielectric layer 22 and the silicon carbide layer are bonded together (fig. 1, col. 4, lines 3-5).

As to claims 16-17, the second dielectric layer may be a silicon oxide formed on a semiconductor layer such as a silicon layer (col. 4, lines 3-5).

As to claim 18, the semiconductor layer may be a silicon germanium (col. 7, line 3).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

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invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Felker, as applied to claim 18 above.

Felker discloses the invention substantially as claimed. However, Felker does not explicitly teach the specific composition of the silicon germanium compound. Nevertheless, it would have been obvious to one skilled in the art at the time the invention was made to construct the composition of SiGe compound of Felker with the specific range for the composition of the SiGe, since it is a prima facie obvious to an artisan for optimization and experimentation to specify the range, as claimed, for the composition of SiGe because applicants have not yet established any criticality for the range.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. (In re Woodruff, 919 F.2d 1575, 1578 (Fed. Cir. 1990).)

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Felker, as applied to claim 14 above, in view of Maa et al. (hereinafter Maa) (6,562,703).

Felker teaches a method of forming a SOI substrate having a semiconductor substrate 12 (fig. 1) with layers 22 (fig. 1) formed on the substrate. The layers are made from silicon oxide, silicon carbide, silicon nitride, silicon germanium, and silicon (fig. 1, col. 7, lines 1-5).

However, Felker does not explicitly disclose that a hydrogen implanted region is included in the semiconductor layer.

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Maa discloses a method of forming a semiconductor device. The method includes the steps of forming a Si substrate 102 (fig. 1); forming a silicon layer 104 (fig. 1); forming a semiconductor layer 106, $\text{Si}_{1-x}\text{Ge}_x$ where x varies from .2-.3 (col. 3, lines 15); forming a silicon oxide layer 107 ; implanting a hydrogen 108 (fig. 1; col. 2, line 8); and implanting additional semiconductor layer 114 and dielectric layer 116 (fig. 1).

Felker and Maa are in the same field of forming a SOI substrate in a semiconductor device.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the semiconductor layer of Felker with a hydrogen implanted region, as taught by Maa, so as to provide a smooth and relaxed film for use in high speed FET applications (Maa, col. 1, lines 55-59).

Note that Maa discloses an overlapping range for the SiGe composition.

8. Claims 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu et al. (hereinafter Hu) (6,413,802) in view of Felker.

Hu discloses a method for forming a SOI device. The method includes the steps of forming a SOI substrate 10 (fig. 2B) with a dielectric layer 12, a semiconductor layer 14 and a dielectric layer 16 (fig. 2B) and a semiconductor layer 18 (fig. 2B). The method also includes the steps of patterning a FinFET body 34 (fig. 2B) from the semiconductor layer, wherein the FinFET has a source (fig. 3) and a drain region (fig. 3) joined by a channel (fig. 3); forming a gate (fig. 2F) around the channel (fig. 2F); and forming a gate insulator 32 (fig. 3) around at least a channel region (fig. 3).

However, Hu does not explicitly teach that the method includes a silicon carbide layer.

Felker teaches a method of forming a SOI substrate having a semiconductor substrate 12 (fig. 1) with layers 22 (fig. 1) formed on the substrate. The layers are made from silicon oxide, silicon carbide, silicon nitride, silicon, and silicon germanium (fig. 1, col. 7, lines 1-5).

Hu and Felker are in the same field of making a SOI substrate in a semiconductor device.

Therefore, as to claims 21-22 and 25-26, it would have been obvious to one skilled in the art at the time the invention was made to modify the invention of Hu with a silicon carbide layer, as taught by Felker, so as to provide an alternative layer material on the SOI substrate.

As to claim 23, although Felker does not explicitly teach that the composition of SiGe. Nevertheless, it would have been obvious to one skilled in the art at the time the invention was made to construct the composition of SiGe compound of Felker with the specific range for the composition of the SiGe, since it is a prima facie obvious to an artisan for optimization and experimentation to specify the range, as claimed, for the composition of SiGe because applicants have not yet established any criticality for the range.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. (In re Woodruff, 919 F.2d 1575, 1578 (Fed. Cir. 1990).)

As to claim 24, Hu discloses that the strained silicon is grown on the FinFET body prior to the gate insulator 44 (col. 4, line 35, and col. 5, lines 2-6).

9. Claims 27-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over White, Jr. et al. (hereinafter White) (6,130,102) in view of Felker.

White discloses a method for forming a SOI device. The method includes the steps of forming a SOI substrate 12 (fig. 5, col. 3, line 30) with a dielectric layer 18, a semiconductor layer 20, and a dielectric layer 28 (fig. 5). Furthermore, the method comprises the steps of

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forming shallow trench isolations (col. 3, lines 34-45, and fig. 5) that extend through the semiconductor material 12 to the dielectric layer 14 and define an active region of the substrate; and forming a MOSFET in the active region (fig. 5).

However, White does not explicitly teach that the method includes a silicon carbide layer.

Felker teaches a method of forming a SOI substrate having a semiconductor substrate 12 (fig. 1) with layers 22 (fig. 1) formed on the substrate. The layers are made from silicon oxide, silicon carbide, silicon nitride, silicon, and silicon germanium (fig. 1, col. 7, lines 1-5).

White and Felker are in the same field of making a SOI substrate in a semiconductor device.

Therefore, as to claims 27-28 and 30-32, it would have been obvious to one skilled in the art at the time the invention was made to modify the invention of White with a silicon carbide layer, as taught by Felker, so as to provide an alternative layer material on the SOI substrate.

As to claim 29, although Felker does not explicitly teach that the composition of SiGe. Nevertheless, it would have been obvious to one skilled in the art at the time the invention was made to construct the composition of SiGe compound of Felker with the specific range for the composition of the SiGe, since it is a prima facie obvious to an artisan for optimization and experimentation to specify the range, as claimed, for the composition of SiGe because applicants have not yet established any criticality for the range.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. (In re Woodruff, 919 F.2d 1575, 1578 (Fed. Cir. 1990).)

Response to Arguments

10. Applicant's arguments filed March 10, 2005, have been fully considered but they are not persuasive.

Applicant argues the rejection of claim 14, because Felker does not teach a particular of a SOI substrate. On the contrary, as stated in the above rejection, the examiner notes that Felker discloses a method of forming a silicon substrate, then forming a dielectric layer, thereby making a SOI substrate. Further, Felker teaches the step of forming a silicon carbide and then forming a second dielectric layer. Moreover, in applicant's remarks on page 7, lines 4-5, applicant fails to claim the specific limitation, as described. In particular, applicant states that "bonding in which layers are grown on separate structures and then bonded through direct contact and thermal treatment". Therefore, Felker still meets the newly amended claim 14.

With respect to claim 20, Felker lacks the teaching of a hydrogen implanted region included in the semiconductor layer. However, Maa discloses an analogous method of forming a semiconductor device having the step as claimed. Therefore the rejection is maintained.

Regarding to claims 21-26, the obviousness rejection over Hu in view of Felker. Hu lacks the method including a silicon carbide layer. Felker cures Hu by discloses an analogous method a SOI substrate with layers are made from silicon oxide, silicon carbide, silicon nitride, silicon, and silicon germanium (fig. 1, col. 7, lines 1-5). Therefore, as to claims 21-22 and 25-26, it would have been obvious to one skilled in the art at the time the invention was made to modify the invention of Hu with a silicon carbide layer, as taught by Felker, so as to provide an alternative layer material on the SOI substrate.

As to claim 27-32, the obviousness rejection over White in view of Felker White lacks a teaching of a silicon carbide layer. Felker cures White by disclosing an analogous method of forming a SOI substrate with layers are made from silicon oxide, silicon carbide, silicon nitride, silicon, and silicon germanium (fig. 1, col. 7, lines 1-5). Therefore, as to claims 27-28 and 30-32, it would have been obvious to one skilled in the art at the time the invention was made to modify the invention of White with a silicon carbide layer, as taught by Felker, so as to provide an alternative layer material on the SOI substrate.

For the foregoing reasons, the rejections are maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The

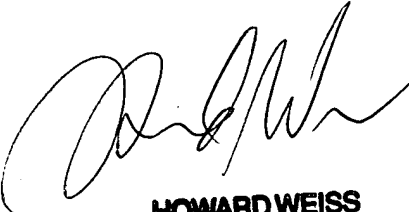
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Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.

Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at <http://www.uspto.gov/ebc/index.html> or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Vikki Trinh,
Patent Examiner
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HOWARD WEISS
PRIMARY EXAMINER